

IN THE CLAIMS:

1-7. (Canceled)

8. (Previously presented) A voting component comprising:

- a current center sample input node that receives a current center sample;
- a current edge sample input node that receives a current edge sample;
- a previous center sample input node that receives a previous center sample;
- an early output node that selectively draws a reference current according to the current center sample, the current edge sample, and the previous center sample;
- a late output node that selectively draws the reference current according to the current center sample, the current edge sample, and the previous center sample;
- circuitry for selectively controlling the early output node and the late output node;
- a complement center sample node that receives a logical complement of the current center sample;
- a complement edge sample node that receives a logical complement of the current edge sample; and
- a complement previous center sample node that receives a logical compliment of the previous center sample.

9 and 10. (Canceled)

11. (Previously presented) The voting component of claim 8, wherein the circuitry comprises:

- a first transistor having a drain connected to the late output node and a gate connected to the complement previous center sample node;
- a second transistor having a drain connected to a source of the first transistor and a gate connected to the current edge sample input node;
- a third transistor having a drain connected the early output node and a gate connected to VDD;

a fourth transistor having a drain connected to a source of the third transistor and a gate connected to the complement edge sample node;

a fifth transistor having a drain connected to a source of the second transistor and a source of the fourth transistor and a gate connected to the current center sample input node;

a sixth transistor having a drain connected to the late output node and a gate connected to the previous center sample input node;

a seventh transistor having a drain connected to a source of the sixth transistor and a gate connected to the complement edge sample node;

an eighth transistor having a drain connected to the early output node and a gate connected to VDD;

a ninth transistor having a drain connected to a source of the eighth transistor and a gate connected to the current edge sample input node;

a tenth transistor having a drain connected to a source of the seventh transistor and a source of the ninth transistor and a gate connected to the complement center sample node; and

a reference current circuit connected to a source of the fifth transistor and a source of the tenth transistor that draws the reference current from the early output node or the late output node according to the current center sample, the current edge sample, and the previous center sample.

12. (Previously presented) The voting component of claim 8, wherein the circuitry comprises an inverter generates the logical complement of the current center sample from the current center sample.

13. (Original) The voting component of claim 8, wherein the early output node selectively draws a reference current based on a logical expression of the current center sample XORed with the current edge sample.

14. (Previously presented) A clock recovery device comprising:
a sample component that obtains center and edge samples of a serial data stream;

a number of voting components that identify early and late operation for a set of consecutive bit times of the serial data stream from the obtained center and edge samples and selectively draw a reference current at early and late output nodes according to the identified operation;

an analyzer that measures and compares current drawn by the number of voting components at the early and late output nodes and indicates an average operation based upon the comparison;

a data clock and a transition clock, wherein the sample component employs the data clock to obtain center samples and the transition clock to obtain edge samples; and

wherein the analyzer component adjusts operation of the data clock and the transition clock according to the average operation of the set of consecutive bit times.

15. (Original) The device of claim 14, wherein the analyzer comprises:

a composite early node connected to the early output nodes of the number of voting components;

a composite late node connected to the late output nodes of the number of voting components;

a first resistor having a first terminal connected to VDD and a second terminal connected to the composite early node;

a second resistor having a first terminal connected to VDD and a second terminal connected to the composite late node;

a third resistor having a first terminal connected to the composite early node;

a composite early plus node connected to a second terminal of the third resistor;

a fourth resistor having a first terminal connected to the composite late node;

a composite late plus node connected to a second terminal of the fourth resistor;

a first reference current circuit connected to the composite early plus node that draws a half of the reference current;

a second reference current circuit connected to the composite late plus node that draws a half of the reference current;

a first comparator that compares a voltage of the composite early node to a voltage of the composite late plus node and generates an early output on the voltage of the composite early node being less than the voltage of the composite late plus node; and

a second comparator that compares a voltage of the composite plus early node to a voltage of the composite late node and generates a late output on the voltage of the composite late node being less than the voltage of the composite early plus node, wherein the early output and the late output indicate the average operation of the set of consecutive bit times.

16. (Canceled)

17. (Previously presented) The device of claim 15, wherein the voting components respectively comprise:

a current center sample input node that receives a current center sample;

a current edge sample input node that receives a current edge sample;

a previous center sample input node that receives a previous center sample;

an early output node that selectively draws a reference current according to the current center sample, the current edge sample, and the previous center sample;

a late output node that selectively draws the reference current according to the current center sample, the current edge sample, and the previous center sample;

a complement center sample node that receives a logical complement of the current center sample;

a complement edge sample node that receives a logical complement of the current edge sample;

a complement previous center sample node that receives a logical complement of the previous center sample

a first transistor having a drain connected to the early output node and a gate connected to the complement previous center sample node;

a second transistor having a drain connected to a source of the first transistor and a gate connected to the current edge sample input node;

a third transistor having a drain connected to the late output node and a gate connected to VDD;

a fourth transistor having a drain connected to a source of the third transistor and a gate connected to the complement edge sample node;

a fifth transistor having a drain connected to a source of the second transistor and a source of the fourth transistor and a gate connected to the current center sample input node;

a sixth transistor having a drain connected to the early output node and a gate connected to the previous center sample input node;

a seventh transistor having a drain connected to a source of the sixth transistor and a gate connected to the complement edge sample node;

an eighth transistor having a drain connected to the late output node and a gate connected to VDD;

a ninth transistor having a drain connected to a source of the eighth transistor and a gate connected to the current edge sample input node;

a tenth transistor having a drain connected to a source of the seventh transistor and a source of the ninth transistor and a gate connected to the complement center sample node; and

a third reference current circuit connected to a source of the fifth transistor and a source of the tenth transistor that draws the reference current from the early output node and the late output node according to the current center sample, the current edge sample, and the previous center sample.

18-23. (Canceled)